Notice of Allowability	Application No.	Applicant(s)	
	09/832,199	KIM, CHUL-MIN	
	Examiner	Art Unit	
	Christopher Onuaku	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *9/13/06*.

2. ☒ The allowed claim(s) is/are *1-23*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 6/22/06
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-23 are allowable over the prior art of record.

2. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 1, the invention relates to a video signal processing integrated circuit (IC), including a method for designing a de-emphasis circuit for a video signal processing IC in order to reduce operating steps and material costs by minimizing the number of components of external application circuits of a de-emphasis output terminal of the video signal processing IC, and an IC made by the method.

The closest references Nonaka et al (US 5,872,605) disclose a video signal processing apparatus, which includes an equalizer for delaying an input color signal by an adjustable phase retardation, made into an integrated circuit, and Kitamura et al (US 5,132,806) teach semiconductor integrated circuit devices, including techniques which are effective when applied to a semiconductor integrated circuit device for use in a color video tape recorder (VTR).

However, Nonaka et al and Kitamura et al fail to explicitly disclose a method of designing a video signal processing integrated circuit (IC), where the method further comprises the steps of incorporating a circuit element for determining a level of a reproduced video signal of the de-emphasis circuit into the video signal processing IC

and connecting the circuit element to a ground which is used exclusively for the luminance signal processing block.

Regarding claim 7, the invention relates to a video signal processing integrated circuit (IC), including a method for designing a de-emphasis circuit for a video signal processing IC in order to reduce operating steps and material costs by minimizing the number of components of external application circuits of a de-emphasis output terminal of the video signal processing IC, and an IC made by the method.

The closest references Nonaka et al (US 5,872,605) disclose a video signal processing apparatus, which includes an equalizer for delaying an input color signal by an adjustable phase retardation, made into an integrated circuit, and Kitamura et al (US 5,132,806) teach semiconductor integrated circuit devices, including techniques which are effective when applied to a semiconductor integrated circuit device for use in a color video tape recorder (VTR).

However, Nonaka et al and Kitamura et al fail to explicitly disclose a video signal processing integrated circuit, where the integrated circuit incorporates a determining circuit for determining a level of a reproduced video signal of a de-emphasis circuit, wherein the determining circuit includes a reproduced video level setting unit.

Regarding claim 11, the invention relates to a video signal processing integrated circuit (IC), including a method for designing a de-emphasis circuit for a video signal processing IC in order to reduce operating steps and material costs by minimizing the

number of components of external application circuits of a de-emphasis output terminal of the video signal processing IC, and an IC made by the method.

The closest references Nonaka et al (US 5,872,605) disclose a video signal processing apparatus, which includes an equalizer for delaying an input color signal by an adjustable phase retardation, made into an integrated circuit, and Kitamura et al (US 5,132,806) teach semiconductor integrated circuit devices, including techniques which are effective when applied to a semiconductor integrated circuit device for use in a color video tape recorder (VTR).

However, Nonaka et al and Kitamura et al fail to explicitly disclose a method of designing a video signal processing integrated circuit (IC), where the method further comprising the steps of incorporating a determining circuit for determining a level of a reproduced video signal of a de-emphasis circuit into the video signal processing IC, and connecting the determining circuit between an output of the de-emphasis circuit and a ground exclusively used for the luminance signal processing block.

Regarding claim 17, the invention relates to a video signal processing integrated circuit (IC), including a method for designing a de-emphasis circuit for a video signal processing IC in order to reduce operating steps and material costs by minimizing the number of components of external application circuits of a de-emphasis output terminal of the video signal processing IC, and an IC made by the method.

The closest references Nonaka et al (US 5,872,605) disclose a video signal processing apparatus, which includes an equalizer for delaying an input color signal by

an adjustable phase retardation, made into an integrated circuit, and Kitamura et al (US 5,132,806) teach semiconductor integrated circuit devices, including techniques which are effective when applied to a semiconductor integrated circuit device for use in a color video tape recorder (VTR).

However, Nonaka et al and Kitamura et al fail to explicitly disclose a video signal processing circuit, where the circuit incorporates a determining circuit for determining a level of a reproduced video signal of a de-emphasis circuit, and a video level setting unit connected between the output of the de-emphasis circuit and a ground which is used exclusively for luminance signal processing.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher Onuaku whose telephone number is 571-272-7379. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Groody can be reached on 571-272-7950. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

COO

9/21/06

James J. Groody
Supervisory Patent Examiner
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